REMARKS

Applicants respectfully request that the Examiner reconsider the subject application as amended herein.

35 U.S.C. §102(a) REJECTION

The Examiner has rejected claims 1, 2, 4-8, 10, 11, 12, 14-19, 21, 23-26, 28, 29, 31, 32, 34-38, 40-43, and 45-51 under 35 U.S.C. §102(b) as being anticipated by "Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs" by Ohsawa et al. (hereafter Ohsawa). Applicants traverse.

Claim 1

In order to support an "anticipation" rejection under §102, a single prior art reference must show each and every element recited in the claims. In this case, claim 1 recites a "memory device" having "a plurality of dynamically refreshable memory cells" and "one or more dynamically changeable use registers." Ohsawa does not describe a memory device having such elements.

In rejecting claim 1, the Office Action cites Ohsawa's DRAM controller and its "refresh flag." Ohsawa in sec. 3.1 third paragraph, describes that the DRAM controller, and not a memory device, provides a refresh flag per row, the DRAM controller not including "a plurality of dynamically refreshable memory cells" as recited in claim 1. Accordingly, the reference does not describe each and every element recited in claim 1, and therefore does not properly support a §102 rejection.

Therefore Applicants respectfully submit that claim 1 includes elements that are not described by Ohsawa. Claim 1 is therefore patentable over Ohsawa.

Applicants respectfully request that the §102 (e) rejection of claim 1 be withdrawn and claim 1 be allowed.

Claims 2, 4-8, and 10

Dependent claims 2, 4-8, and 10 are allowable by virtue of their dependency on respective base claim 1, as well as for the additional limitations they contain.

For instance, claim 2 recites the memory device of claim 1 further comprising "self-refresh logic on the memory device wherein the self-refresh logic is configured to not refresh the indicated unused memory cells." The Examiner has commented that Ohsawa sec. 4.3 mentions "static mode which is the claimed self-refresh mode." Applicants respectfully traverse. The "static mode" described in Ohsawa section 4.3 is when a DRAM keeps memory by performing refreshes as a consequence of operations e.g. I/O operations and interrupt operations (Ohsawa sec. 4.3 paragraph 6, sentence 2). This static mode is not "wherein the self-refresh logic is configured to not refresh the indicated unused memory cells" as recited in claim 2. For this additional reason, claim 2 is allowable over Ohsawa.

As another example, claims 10 refers to the registers comprising bits that correspond to a page of memory cells. The Office Action comments that a page of memory cells is the same as a row of memory cells. Applicants traverse. A row refers to a dimension of a two-dimensional memory organization, the second dimension commonly termed a column. Generally a row and a column are each separately addressable in a memory cell access. A page on the other hand is a section of memory cells that are accessible at one time and treated as a unit of data. A page may represent a group of memory cells other than all cells of a row.

Accordingly, for any of these reasons, the reference does not describe each and every element recited in claims 2, 4-8, and 10, and therefore does not properly support a §102 rejection.

Therefore Applicants respectfully submit that claims 2, 4-8, and 10 are patentable over Ohsawa. Applicants respectfully request that the §102(e) rejection of claims 2, 4-8, and 10 be withdrawn.

Claim 11

Claim 11 recites a "memory device" having "a plurality of refreshable memory cells" and "one or more dynamically changeable use registers corresponding to groups of one or more memory cells." Ohsawa does not describe a memory device having such elements.

As described with reference to claim 1, the Office Action cites Ohsawa's DRAM controller and its "refresh flag" (Ohsawa section 3.1 third paragraph, and FIG. 5). However, Ohsawa's DRAM controller does not include "a plurality of refreshable memory cells" as recited in claim 11. Accordingly, the reference does not describe each and every element recited in claim 11, and therefore does not properly support a §102 rejection. Therefore, Applicants respectfully submit that claim 11 includes elements that are not described by Ohsawa. Claim 11 is therefore patentable over Ohsawa. Applicants respectfully request that the §102 (e) rejection of claim 1 be withdrawn and claim 11 be allowed.

Claims 12 and 14-18

Dependent claims 12, and 14-18, are allowable by virtue of their dependency on respective base claim 11, as well as for the additional limitations they contain.

For instance, claim 12 recites the memory device further comprising self-refresh logic on the memory device, wherein the self-refresh logic is configured not to refresh unused memory cells. The Examiner comments that Ohsawa sec. 4.3 mentions "static mode which is the claimed self-refresh mode." As described with reference to claim 2, the "static mode" described in Ohsawa section 4.3 is when a DRAM keeps memory by performing refreshes as a consequence of operations. This static mode is not "wherein the self-refresh logic is configured to not refresh the indicated unused memory cells" as recited in claim 12. For this additional reason, claim 12 is allowable over Ohsawa.

Accordingly, for any of these reasons claims 12 and 14-18 are patentable over Ohsawa. Applicants respectfully request that the §102(e) rejection of claims 12 and 14-18 be withdrawn.

Claim 19

Claim 19 recites a system having "recent-access flags associated with the memory cells, the recent access flags being configurable to indicate whether corresponding memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval."

Ohsawa does not disclose, teach, or suggest a system comprising recent-access flags associated with the memory cells, the recent-access flags configurable to indicate whether the corresponding memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, as recited in claim 19. Furthermore, the Office Action does not acknowledge this element of claim 19 and does not attempt to show its presence in the cited prior art. Ohsawa clearly states (Ohsawa sec. 3.1 third paragraph) that the load and store operations

are initiated from the processor, and clearly does not disclose anything resembling the recited "recent-access flags." Accordingly, the reference does not describe each and every element recited in claim 19, and therefore does not properly support a §102 rejection.

Therefore, Applicants respectfully submit that claim 19 includes elements that are not described by Ohsawa. Claim 19 is therefore patentable over Ohsawa. Applicants respectfully request that the §102 (e) rejection of claim 19 be withdrawn and claim 19 be allowed.

Claims 21, and 23-24

Dependent claims 21, and 23-24 are allowable by virtue of their dependency on respective base claim 19, as well as for the additional limitations they contain.

For instance, claim 23 recites that the use registers are on the memory devices. As described with reference to claim 1, Ohsawa in sec. 3.1 third paragraph describes instead a system in which the refresh flag is on the DRAM controller

Accordingly, for any of these reasons claims 21, and 23-24 are patentable over Ohsawa. Applicants respectfully request that the §102(e) rejection of claims 21, and 23-24 be withdrawn.

Claim 25

Claim 25 recites a system wherein the memory controller is responsive to the operating system to operate non-allocated memory at reduced power.

Ohsawa does not describe operating the non-allocated memory at a reduced power as recited by the Applicants above. The Office Action does not show this element in the cited art.

Therefore Applicants respectfully submit that claim 25 includes elements that are not described by Ohsawa. Claim 25 is therefore patentable over Ohsawa. Applicants respectfully request that the §102 (e) rejection of claim 25 be withdrawn and claim 25 be allowed.

Claims 26, 28-29, and 31

Dependent claims 26, 28-29, and 31 are allowable by virtue of their dependency on respective base claim 25, as well as for the additional limitations they contain. Applicants respectfully request that the §102(e) rejection of claims 26, 28-29, and 31 be withdrawn.

Claim 32

Claim 32 recites a method comprising determining which rows have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval.

Ohsawa does not disclose, teach, or suggest determining which rows have been accessed in a manner that refreshed the memory cells during a previous refresh cycle, as, as recited by Applicants. Ohsawa clearly states in sec. 3.1 third paragraph that the load and store operations are initiated from the processor. Furthermore, the Office Action does not acknowledge this element of claim 32 and does not attempt to show its presence in the cited prior art. Accordingly, the reference does not describe each and every element recited in claim 32, and therefore does not properly support a §102 rejection.

Therefore Applicants respectfully submit that claim 32 includes elements that are not described by Ohsawa. Claim 32 is therefore patentable over Ohsawa. Applicants respectfully request that the §102 (e) rejection of claim 32 be withdrawn and claim 32 be allowed.

Claims 34 and 35

Dependent claims 34 and 35 are allowable by virtue of their dependency on respective base claim 32, as well as for the additional limitations they contain. Applicants respectfully request that the §102(e) rejection of claims 21, and 23-24 be withdrawn.

Claim 38

Claim 38 recites a memory controller configured to perform actions comprising keeping track of which memory cells have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval.

Ohsawa does not disclose, teach, or suggest a system comprising keeping track of which memory cells have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval. Furthermore, the Office Action does not acknowledge this element of claim 38 and does not attempt to show its presence in the cited prior art. As described with reference to claim 19, Ohsawa clearly states that the load and store operations are initiated from the processor.

Therefore Applicants respectfully submit that claim 1 includes elements that are not described by Ohsawa. Claim 38 is therefore patentable over Ohsawa. Applicants respectfully request that the §102 (e) rejection of claim 38 be withdrawn and claim 38 be allowed.

Claim 40

Dependent claim 40 is allowable by virtue of its dependency on respective base claim 40, as well as for the additional limitations it contains. Applicants respectfully request that the §102(e) rejection of claim 40 be withdrawn.

THE 35 U.S.C. §103 REJECTION

The Examiner has rejected claims 3, 9, 13, 20, 22, 27, 30, 33, 39, 44, 47, 50, 51, 52, and 53 under U.S.C. §103(a) as being unpatentable over Ohsawa. Applicants traverse.

Claims 3 and 9

Dependent claims 3 and 9 are allowable by virtue of their dependency on respective base claim 1, as well as for the additional limitations they contain.

Claim 3 recites the memory device of claim 1, further comprising recent-access flags associated with respective sets of the memory cells, being configured to indicate whether the associated sets of memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, the memory device configured to omit refreshing memory cells that are indicated by the recent-access flags to have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval.

The Office Action comments that the cited art does not disclose the recent access flags. The Office Action states that it would have been obvious at the time the invention was made to include the recent access flags because Ohsawa's goal is to have the fewest refresh cycles possible. Ohsawa mentions these reads and writes as loads and stores at section 3.1 third paragraph.

Ohsawa does not disclose, teach, or suggest recent access flags. Ohsawa clearly states in the section that the Examiner cites (Ohsawa sec. 3.1 third paragraph) that the load and store operations are initiated from the processor. The processor does not understand whether the load and store commands will require an activate operation to be performed by the DRAMs, so cannot indicate whether the corresponding memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval as recited in claim 3.

The Examiner comments that it would be obvious but has provided nothing from the prior art to support his assertions. Having a goal of doing something is not the same as having a way to do it. In this case we have provided a specific novel way to accomplish the goal, and there is nothing in the prior art that would have suggested this specific way. As shown above, the load and store operations cannot indicate whether the associated sets of memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval. Moreover, there must be some suggestion or motivation in the references or in knowledge generally available to one of ordinary skill in the art to modify the references. The teaching or suggestion to make the claimed combination must be found in the prior art and not in the applicant's disclosure (MPEP, section 2142, 2100-108 (Rev. 3). Applicants respectfully submit that this is an example of impermissible hindsight.

Claim 9 defines the memory device recited in claim 1 wherein the use registers comprise bits that correspond to a ~~page~~ bank of memory cells. The Office Action comments that Ohsawa's refresh flags refer to rows, and therefore not the ~~page~~ bank recited ion claim 9. The Office Action states that it would have been obvious

to use refresh flags for a bank because this would allow an entire bank to be shutdown, avoiding the need to read the refresh flag of each row. Having a goal of doing something is not the same as having a way to do it. In this case we have provided a specific novel way to accomplish the goal, and there is nothing in the prior art that would have suggested this specific way. Moreover, there must be some suggestion or motivation in the references or in knowledge generally available to one of ordinary skill in the art to modify the references. The teaching or suggestion to make the claimed combination must be found in the prior art and not in the applicant's disclosure (MPEP, section 2142, 2100-108 (Rev. 3) Applicants respectfully submit that this is an example of impermissible hindsight.

Therefore Applicants respectfully submit that claims 3 and 9 are each unpatentable over Ohsawa. Applicants respectfully request that the §103 (a) rejection of claim 3 and claim 9 be withdrawn and claim 3 and claim 9 each be allowed.

Claim 13

Dependent claim 13 is allowable by virtue of its dependency on respective base claim 11, as well as for the additional limitations it contains.

Claim 13 recites the memory device of claim 11 including recent-access flags associated with respective sets of the memory cells configured to indicate whether the associated sets of memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, the memory device configured to omit refreshing of memory cells indicated by the recent-access flags to have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval.

The Office Action comments that the cited art does not disclose the recent access flags. The Office Action states that it would have been obvious at the time the invention was made to include the recent access flags because Ohsawa's goal is to have the fewest refresh cycles possible. Ohsawa mentions these reads and writes as loads and stores at section 3.1 third paragraph.

As described with respect to claim 3, Ohsawa does not disclose, teach, or suggest recent access flags. Ohsawa clearly states that the load and store operations are initiated from the processor, which cannot indicate whether the corresponding memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval as recited in claim 13.

The Examiner comments that it would be obvious but has provided nothing from the prior art to support his assertions. Having a goal of doing something is not the same as having a way to do it. Applicants have provided a specific novel way to accomplish the goal, and there is nothing in the prior art that would have suggested this specific way. As shown above, the load and store operations cannot indicate whether the associated sets of memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval. Moreover, there must be some suggestion or motivation in the references or in knowledge generally available to one of ordinary skill in the art to modify the references. The teaching or suggestion to make the claimed combination must be found in the prior art and not in the applicant's disclosure (MPEP, section 2142, 2100-108 (Rev. 3). Applicants respectfully submit that this is an example of impermissible hindsight.

Therefore Applicants respectfully submit that claim 13 is unpatentable over Ohsawa. Applicants respectfully request that the §103 (a) rejection of claim 13 be withdrawn and claim 13 be allowed.

Claims 20 and 22

Dependent claims 20 and 22 are allowable by virtue of their dependency on respective base claim 19, as well as for the additional limitations they contain.

Claim 20 defines a system as recited in claim 19, wherein the memory controller is configured not to refresh those memory cells that are indicated to have been accessed in a manner that refreshed the memory cells during the previous refresh cycle interval.

Regarding claim 20, the Office Action comments that the cited art does not disclose the recent access flags, but states that it would have been obvious at the time the invention was made to include the recent access flags because Ohsawa's goal is to have the fewest refresh cycles possible. Ohsawa mentions these reads and writes as loads and stores at section 3.1 third paragraph.

As described with respect to claim 3, Ohsawa does not disclose, teach, or suggest recent access flags, and more specifically does not disclose, teach, or suggest not refreshing memory cells that are indicated to have been accessed in a manner that refreshed the memory cells during the previous refresh cycle interval. Ohsawa clearly states that the load and store operations are initiated from the processor which cannot indicate not refreshing memory cells accessed in a manner that refreshed the memory cells during the previous refresh cycle interval as recited in claim 20.

The Examiner comments that it would be obvious but has provided nothing from the prior art to support his assertions. Having a goal of doing something is not the same as having a way to do it. Applicants have provided a specific novel way to accomplish the goal, and there is nothing in the prior art that would have suggested this specific way. As shown above, the load and store operations cannot indicate whether the associated sets of memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval. Ohsawa does not disclose, teach, or suggest a memory controller configured to refresh not to refresh those memory cells that are indicated to have been accessed in a manner that refreshed the memory cells during the previous refresh cycle interval. As described with reference to claim 3, Ohsawa clearly states that the load and store operations are initiated from the processor. The processor cannot indicate whether the corresponding memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval as recited by Applicants. Applicants respectfully submit that this is an example of impermissible hindsight.

Therefore Applicants respectfully submit that claims 20 and 22 are each unpatentable over Ohsawa. Applicants respectfully request that the §103 (a) rejection of claims 20 and 22 be withdrawn and claims 20 and 22 each be allowed.

Claims 27 and 30

Dependent claims 27 and 30 are allowable by virtue of their dependency on respective base claim 25, as well as for the additional limitations they contain.

Claim 27 defines a system as recited in claim 25, further comprising the recent-access flags recited as described above with reference to claim 3.

The Office Action comments that the cited art does not disclose the recent access flags. The Office Action states that it would have been obvious at the time the invention was made to include the recent access flags because Ohsawa's goal is to have the fewest refresh cycles possible. Ohsawa mentions these reads and writes as loads and stores at section 3.1 third paragraph.

As described above with reference to claim 3, Ohsawa does not disclose, teach, or suggest recent access flags. Ohsawa clearly states in the section that the Examiner cites that the load and store operations are initiated from the processor, which cannot indicate whether the corresponding memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval as recited in claim 27.

The Examiner comments that it would be obvious but has provided nothing from the prior art to support his assertions. Having a goal of doing something is not the same as having a way to do it. In this case we have provided a specific novel way to accomplish the goal, and there is nothing in the prior art that would have suggested this specific way. As shown above, the load and store operations cannot indicate whether the associated sets of memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval. Moreover, there must be some suggestion or motivation in the references or in knowledge generally available to one of ordinary skill in the art to modify the references. The teaching or suggestion to make the claimed combination must be found in the prior art and not in the applicant's disclosure (MPEP, section 2142, 2100-108 (Rev. 3). Applicants respectfully submit that this is an example of impermissible hindsight.

Therefore Applicants respectfully submit that claims 27 and 30 are each unpatentable over Ohsawa. Applicants respectfully request that the §103 (a) rejection of claims 27 and 30 each be withdrawn and claims 27 and 30 each be allowed.

Claim 33

Dependent claim 33 is allowable by virtue of its dependency on respective base claim 32, as well as for the additional limitations it contains.

Claim 33 recites "omitting refreshing of memory rows that have been accessed in a manner that refreshed the memory cells during the previous refresh cycle."

The Office Action comments that the cited art does not disclose the recent access flags, but states that it would have been obvious at the time the invention was made to include the recent access flags because Ohsawa's goal is to have the fewest refresh cycles possible. Ohsawa mentions these reads and writes as loads and stores at section 3.1 third paragraph.

Ohsawa does not disclose, teach, or suggest recent access flags, and more specifically does not disclose, teach, or suggest omitting refreshing of memory rows that have been accessed in a manner that refreshed the memory cells during the previous refresh cycle. Ohsawa clearly states that the load and store operations are initiated from the processor which cannot omit refreshing memory rows that have been accessed in a manner that refreshed the memory cells during the previous refresh cycle.

The Examiner comments that it would be obvious but has provided nothing from the prior art to support his assertions. Having a goal of doing something is

not the same as having a way to do it. Applicants have provided a specific novel way to accomplish the goal, and there is nothing in the prior art that would have suggested this specific way. As shown above, the load and store operations cannot indicate whether to omit refreshing of memory rows that have been accessed in a manner that refreshed the memory cells during the previous refresh cycle. As described with reference to claim 3, Ohsawa clearly states that the load and store operations are initiated from the processor. The processor cannot indicate omitting refreshing of memory rows that have been accessed in a manner that refreshed the memory cells during the previous refresh cycle as recited by Applicants. Moreover, there must be some suggestion or motivation in the references or in knowledge generally available to one of ordinary skill in the art to modify the references. The teaching or suggestion to make the claimed combination must be found in the prior art and not in the applicant's disclosure (MPEP, section 2142, 2100-108 (Rev. 3). Applicants respectfully submit that this is an example of impermissible hindsight.

Therefore Applicants respectfully submit that claim 33 is unpatentable over Ohsawa. Applicants respectfully request that the §103 (a) rejection of claim 33 be withdrawn and claim 33 be allowed.

Claim 39

Dependent claim 39 is allowable by virtue of its dependency on respective base claim 38, as well as for the additional limitations it contains.

Claim 39 recites the memory controller of claim 38 being configured to perform actions comprising "omitting refreshing of those memory cells that have been accessed in a manner that refreshed the memory cells during the previous

refresh cycle. " For the same reason described with reference to claim 33, Ohsawa does not disclose, teach, or suggest omitting refreshing of memory rows accessed in a manner that refreshed the memory cells during the previous refresh cycle. Therefore Applicants respectfully submit that claim 39 is unpatentable over Ohsawa. Applicants respectfully request that the §103 (a) rejection of claim 39 be withdrawn and claim 39 be allowed.

Claim 52

Claim 52 defines a method comprising:

periodically refreshing memory cells;
keeping track of which memory cells have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval; and
omitting refreshing of those memory cells that have been accessed in a manner that refreshed the memory cells during the previous refresh cycle.

As described with respect to claims 38 Ohsawa does not disclose, teach, or suggest a system comprising keeping track of which memory cells have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, as recited by Applicants. As described with reference to claim 39, Ohsawa does not disclose, teach, or suggest omitting refreshing of memory rows accessed in a manner that refreshed the memory cells during the previous refresh cycle, as recited by Applicants. Therefore Applicants respectfully submit that for either of these reasons, claim 52 is unpatentable over Ohsawa. Applicants respectfully request that the §103 (a) rejection of claim 52 be withdrawn and claim 52 be allowed.

Claim 53

Dependent claim 53 is allowable by virtue of its dependency on respective base claim 52, as well as for the additional limitations it contains. Therefore

Applicants respectfully submit that claim 53 is unpatentable over Ohsawa. Applicants respectfully request that the §103 (a) rejection of claim 53 be withdrawn and claim 53 be allowed.

CONCLUSION

Applicant respectfully requests reconsideration of the rejection of claims 1-35, 38-40, and 52-53 in view of the above remarks. Applicant respectfully suggests that claims 1-35, 38-40, and 52-53 are in condition for allowance.

Should any matter in this case remain unresolved, the undersigned attorney respectfully requests a telephone conference with the Examiner to resolve any such outstanding matter.

Respectfully Submitted,

Date: July 8, 2003

Kenneth Paley
Reg. No. 38,989
(509)324-9256 x217